What is claimed is:

1   1.   A method of fabricating a semiconductor memory

2 device comprising:

3   providing a substrate;

4   sequentially forming a first conductive layer, a

5   first type doped semiconductor layer, a first

6   dielectric layer, a second type doped

7   semiconductor layer on the substrate;

8   patterning the second type doped semiconductor

9   layer, the first dielectric layer, the first

10   type doped semiconductor layer, and the

11   conductive layer along the first direction,

12   thereby turning the conductive layer into a

13   first conductive line;

14   patterning the second type doped semiconductor

15   layer, the first dielectric layer, and the

16   first type doped semiconductor layer into a

17   memory cell;

18   depositing a second dielectric layer overlying the

19   substrate, wherein oxygen plasma sputtering is

20   employed to clean the substrate before

21   deposition;

22   planarizing the second dielectric layer to expose

23   the memory cell; and

24   forming a second conductive line overlying the

25   second dielectric layer, running generally

26   orthogonal to the first conductive line.

1   2.   The method according to claim 1, wherein the

2 first type doped semiconductor layer is a p^+-type doped

3 silicon layer.

1   3.   The method according to claim 1, wherein the

2 first conductive layer comprises a stack of TiN/TiSi$_2$/p$^+$-

3 type doped silicon layers.

1   4.   The method according to claim 1, wherein the

2 first conductive line is a word line.

1   5.   The method according to claim 1, wherein

2   formation of the first dielectric layer comprises rapid

3   thermal oxidation of silicon.

1   6.   The method according to claim 1, wherein the

2   second type doped silicon layer is n-type doped silicon

3   layer.

1   7.   The method according to claim 1, wherein the

2   memory cell comprises a stack of p^{+}-type doped

3   silicon/first dielectric/n-type doped silicon layers.

1   8.   The method according to claim 1, wherein the

2   step of oxygen plasma sputtering is performed using

3   oxygen gas with a flow rate between about 300 and

4   400sccm.

1   9.   The method according to claim 8, wherein the

2   step of oxygen plasma sputtering is performed using argon

3   gas at with a flow rate between about 200 and 250sccm.

1   10. The method according to claim 8, wherein the

2   step of oxygen plasma sputtering is performed at a

3   temperature within a range of about 225 to 275°C.

1   11. The method according to claim 7, wherein the

2   step of oxygen plasma pre-sputtering is performed at a

3   power within a range of about 1000 to 1500W.

1   12. The method according to claim 1, wherein the

2   second conductive layer comprises a stack of n^+-type doped

3   silicon/TiN/$TiSi_2$/n^+-type doped silicon/n-type doped

4   silicon layers.

1   13. The method according to claim 1, wherein the

2   second conductive line is a bit line.

1   14. A method of fabricating one time programmable

2   read only memory (OPTROM) device, comprising:

3   providing a substrate;

4   sequentially forming a stack of p^+-doped silicon

5   layer/titanium silicide/titanium nitride/p^+-

6   doped silicon layer/first dielectric/n-type

7   doped silicon layers on the substrate;

8   patterning the stack of p^+-doped silicon

9   layer/titanium silicide/titanium nitride/p^+-

10   doped silicon layer/first dielectric/n-type

11   doped silicon layers along the first direction,

12   thereby turning the stack of p^+-doped silicon

13   layer/titanium silicide/titanium nitride layers

14   into a word line;

15   patterning the stack of p^+-doped silicon layer/first

16   dielectric/n-type doped silicon layers into a

17   memory cell;

18   depositing a second dielectric layer overlying the

19   substrate, wherein oxygen plasma sputtering is

20   employed   to   clean   the   substrate   before

21   deposition;

22   planarizing   the   second   dielectric   layer   to   expose

23   the memory cell; and

24   forming   a   stack   of n^+-type   doped   silicon/   titanium

25   nitride/   titanium   silicide   /n^+-type   doped

26   silicon/n-type   doped   silicon   layers   over   the

27   second   dielectric   layer   and   patterning   the   same

28   into   a   bit   line,   running   generally

29   perpendicular to the word line.

1   15.   The   method   according   to   claim   14,   wherein

2   formation   of   the   first   dielectric   layer   comprises   rapid

3   thermal oxidation of silicon oxide.

1   16.   The   method   according   to   claim   14,   wherein   the

2   step   of   oxygen   plasma   sputtering   is   performed   using

3   oxygen   gas   with   a   flow   rate   between   about   300   and

4   400sccm.

1   17. The method according to claim 14, wherein the

2   step of oxygen plasma sputtering is performed using argon

3   gas with a flow rate between about 200 and 250sccm.

1   18. The method according to claim 14, wherein the

2   step of oxygen plasma sputtering is performed at a

3   temperature within a range of about 225 to 275°C.

1   19. The method according to claim 14, wherein the

2   step of oxygen plasma pre-sputtering is performed at a

3   power within a range of about 1000 to 1500W.

1   20.   A semiconductor memory device comprising:

2   a first conductive line disposed on a semiconductor

3   substrate, the surface of the first conductive

4   line being substantially silicon residue free;

5   a   second   conductive   line   running   generally

6   perpendicular to the first conductive line;

7   a memory cell between the first line and the second

8   line; and

9   a dielectric layer, surrounding the memory cell;

10   wherein the surface of the first conductive line is

11   oxygen   plasma   sputtered   for   preventing

12   accumulation of silicon residue.

1   21.   The   semiconductor   memory   device   according   to

2   claim 20, wherein the first conductive line is word line

3   and the second conductive line is bit line.

1   22.   The   semiconductor   memory   device   according   to

2   claim 20, wherein the first conductive line comprises a

3   stack of $TiN/TiSi_2/p^+$-type doped silicon layers.

1   23. The semiconductor memory device according to

2   claim 20, wherein the memory cell comprises a stack of p^+-

3   doped silicon layer/first dielectric/n-type doped silicon

4   layers.

1   24. The semiconductor memory device according to

2   claim 20, wherein formation of the first dielectric layer

3   comprises rapid thermal oxidation of silicon oxide.

1   25. The semiconductor memory device according to

2   claim 20, wherein the second conductive layer comprises a

3   stack of n^+-type doped silicon/TiN/$TiSi_2$/n^+-type doped

4   silicon/n-type doped silicon layers.